

**LAB MANUAL**

**EDA Workshop**

**(ECW 205B)**

**PREPARED BY: MEENAKSHI GUPTA**

**FOR**

**IV SEMESTER CSE**

***Department of Electronics & Communication Engg.***

***MANAV RACHNA UNIVERSITY***

***SECTOR-43, FAR I D A B A D – 121001***

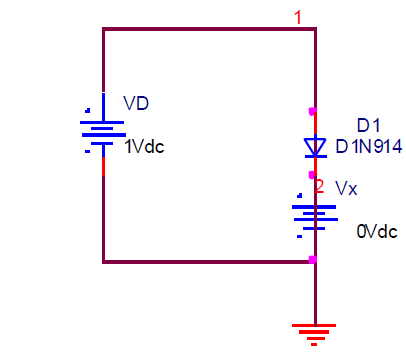
**LIST OF EXPERIMENTS**

1. Simulate and study V-I characteristics of a Diode using PSPICE windows.
2. Simulate and study Half-wave and Full-wave Rectifier using PSPICE windows
3. Simulate and study Diode Clipper and Clamper circuit using PSPICE windows.
4. Simulate and study V-I characteristics of a NPN-BJT using PSPICE windows.
5. Simulate and study Darlington pair amplifier circuit using PSPICE windows and determine quiescent condition.
6. Simulate and study transient & frequency response of a BJT amplifier in common- emitter configuration using PSPICE windows.
7. Simulate and study active low-pass, high-pass & band-pass filter using PSPICE windows.
8. Simulate and study Integrator using PSPICE windows.
9. Simulate and study Differentiator using PSPICE windows.
10. Simulate and study basic AND, OR, NOT, NOR, NAND, EX-OR gates using PSPICE windows.

# EXPERIMENT NO 1

**AIM:** Simulate and study V-I characteristics of a Diode using PSPICE windows.

**CIRCUIT DIAGRAM:**

****

**PROGRAM:**

vd 1 0 dc 1v

d1 1 2 d1n914;

vx 2 0 dc 0v;

.model D1N914 D(Is=168.1E-21 N=1 Rs=.1 Ikf=0 Xti=3 Eg=1.11 Cjo=4p M=.3333

+ Vj=.75 Fc=.5 Isr=100p Nr=2 Bv=100 Ibv=100u Tt=11.54n)

.dc vd 0 1v 0.01v;

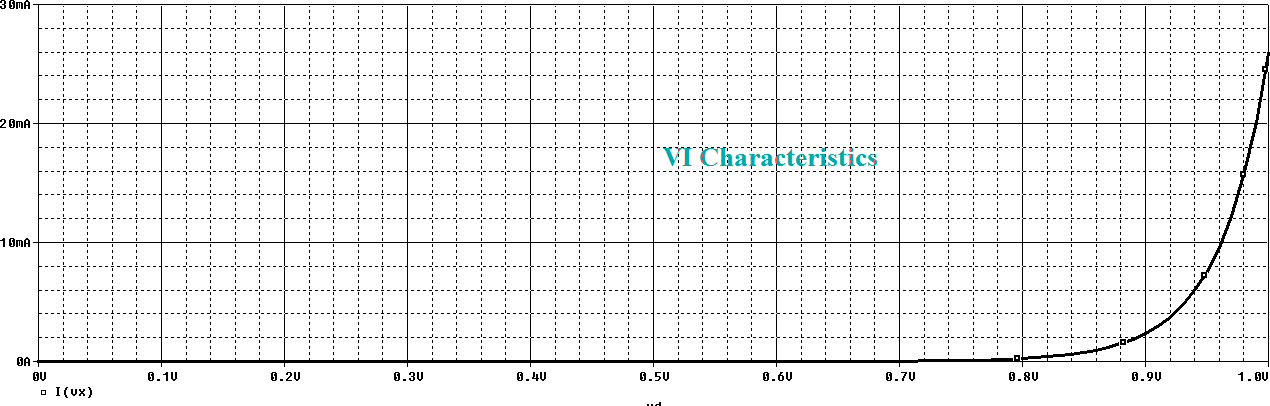
.plot dc I(vx);

.probe;

.tran 0us 100us;

.end;

**RESULT:**

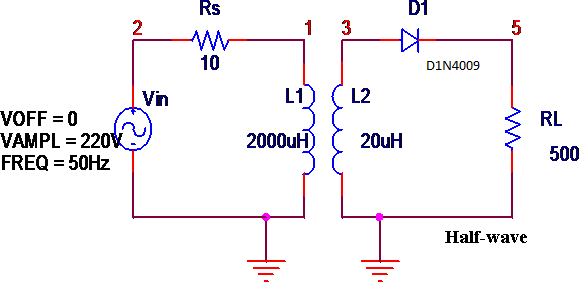


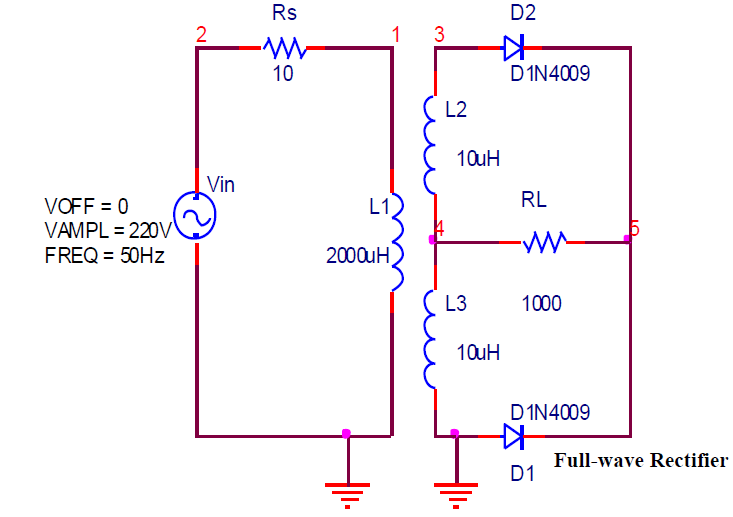
**CONCLUSION:** The forward biased silicon diode in an electronic system under dc condition has a drop of 0.7v across it in conduction state at any value of diode current.

**EXPERIMENT NO 2**

**AIM:** Simulate and study Half-wave and Full-wave Rectifier using PSPICE windows.

**CIRCUIT DIAGRAM:**





## PROGRAM:

\*HALF WAVE rectifier VIN 2 0 sin(0 220V 50HZ)

RL 5 0 500

RS 2 1 10

L1 1 0 2000uH

L2 3 0 20uH

K1 L1 L2 0.99999 D1 3 5 D1N4009

.model D1N4009 D(Is=544.7E-21 N=1 Rs=.1 Ikf=0 Xti=3 Eg=1.11 Cjo=4p M=.3333

+ Vj=.75 Fc=.5 Isr=30.77n Nr=2 Bv=25 Ibv=100u Tt=2.885n)

.tran 0.2m 200m

.plot tran v(3), v(5)

.probe

.end

\*FULL WAVE rectifier Vin 2 0 sin(0 230V 50HZ)

RL 5 4 1000

RS 2 1 10

L1 1 0 2000

L2 3 4 10

L3 4 0 10

K1 L1 L2 L3 0.99 D1 0 5 D1N4009

D2 3 5 D1N4009

.model D1N4009

D(Is=544.7E-21 N=1 Rs=.1 Ikf=0 Xti=3 Eg=1.11 Cjo=4p M=.3333

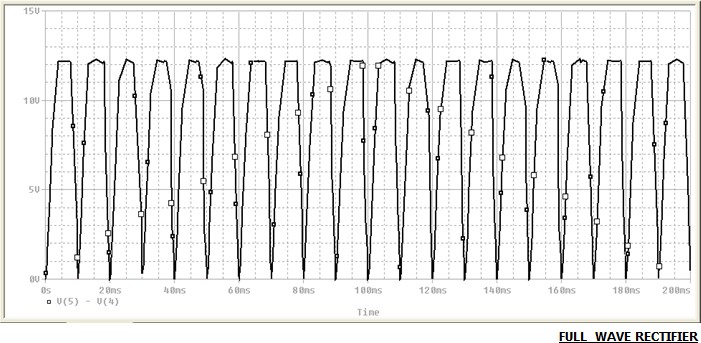
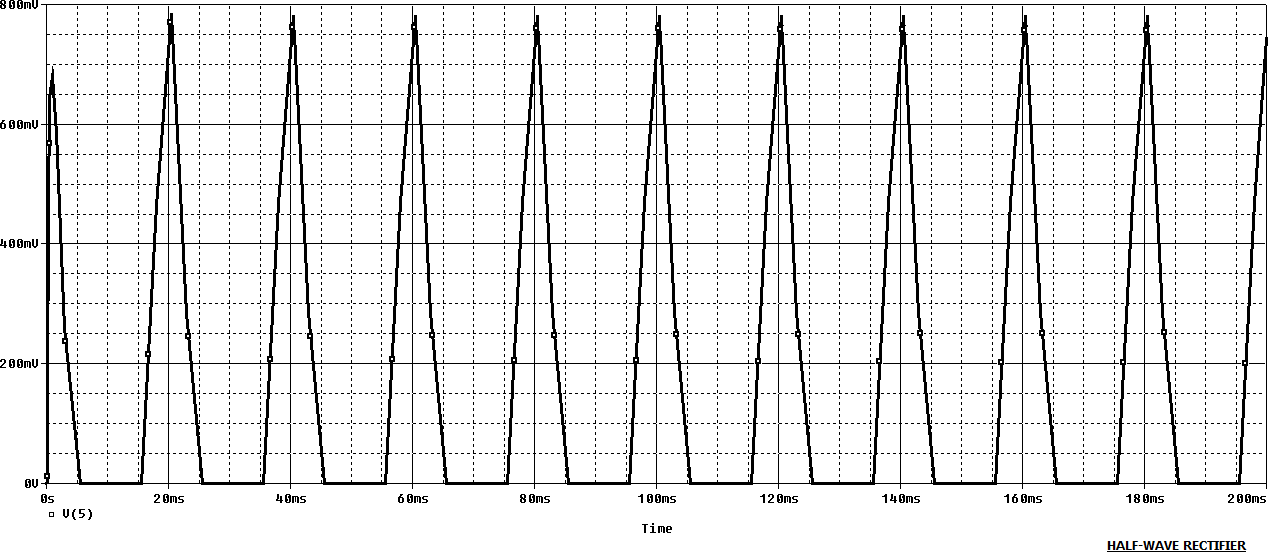
+ Vj=.75 Fc=.5 Isr=30.77n Nr=2 Bv=25 Ibv=100u Tt=2.885n)

.tran 0.2ms 200ms

.probe

.end

**RESULT:**



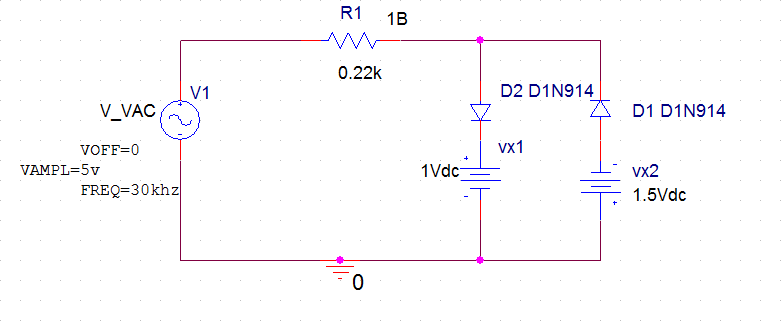
**CONCLUSION:** We are able to visualise the expected output of Half-wave and Full-wave Rectifier circuit as given in theory.

**EXPERIMENT NO 3**

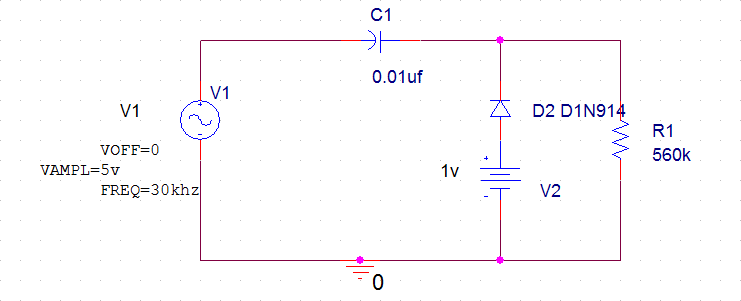
**AIM:** Simulate and study Diode Clipper and Clamper circuit using PSPICE windows.

**CIRCUIT DIAGRAM:**

Clipper Circuit-



Clamper Circuit-



**PROGRAM:**

\*CLIPPER CIRCUIT

V\_VAC 1 0 sin(0 5v 30khz);

r1 1 2 0.22k;

d1 2 3 D1N914;

d2 4 2 D1N914;

vx1 3 0 dc 1v;

vx2 0 4 dc 1.5v;

.model D1N914 D(Is=168.1E-21 N=1 Rs=.1 Ikf=0 Xti=3 Eg=1.11 Cjo=4p M=.3333

+ Vj=.75 Fc=.5 Isr=100p Nr=2 Bv=100 Ibv=100u Tt=11.54n)

.probe;

.tran 0us 100us;

.end;

\*CLAMPER CIRCUIT

V1 1 0 sin(0 5v 30khz);

c1 1 2 0.01u;

d1 3 2 D1N914;

r1 2 0 560k;

v2 3 0 1v;

.model D1N914 D(Is=168.1E-21 N=1 Rs=.1 Ikf=0 Xti=3 Eg=1.11 Cjo=4p M=.3333

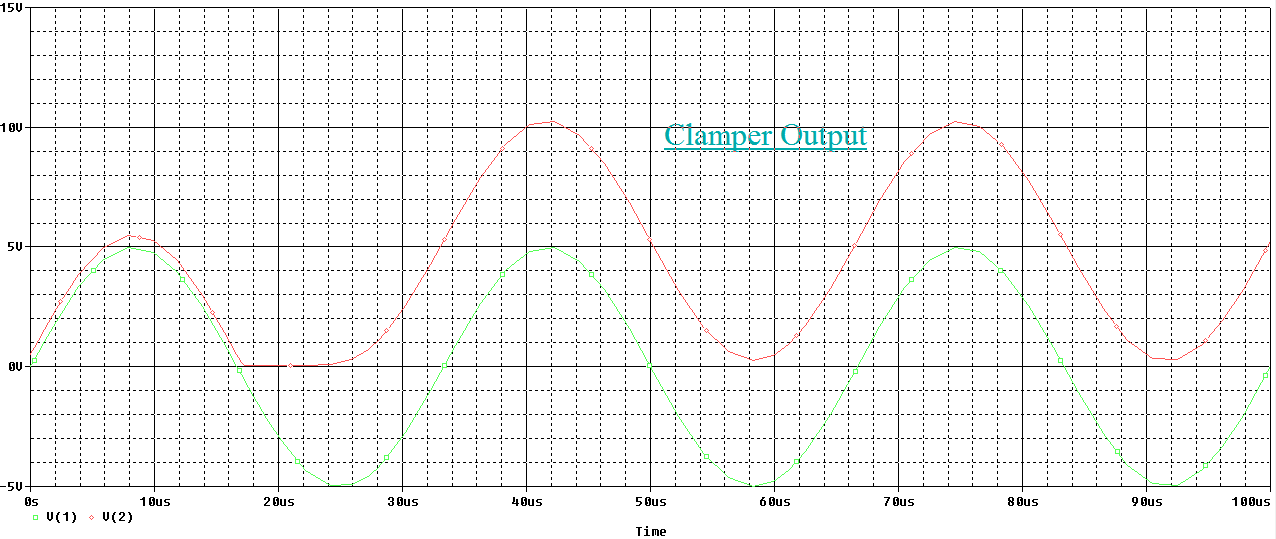
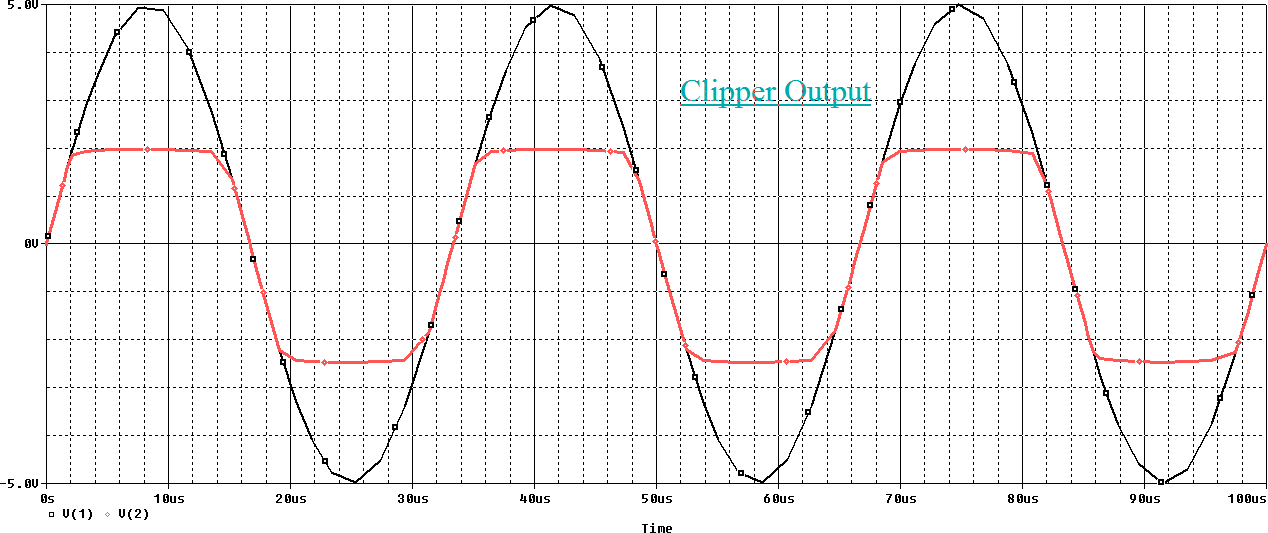
+ Vj=.75 Fc=.5 Isr=100p Nr=2 Bv=100 Ibv=100u Tt=11.54n)

.probe;

.tran 0us 100us;

.end;

**RESULT:**



**CONCLUSION:** We are able to visualise the expected output of Clipper Circuit and Clamper Circuit as given in theory.

**EXPERIMENT NO 4**

**AIM:** Simulate and study V-I characteristics of a NPN-BJT using PSPICE windows.

**CIRCUIT DIAGRAM:**

1

Q1 Q2N2222A

IB

1mAdc

VCE

12Vdc

## PROGRAM:

\* NPN-BJT CHARACTERISTICS IB 0 1 DC 1MA

VCE 2 0 DC 12V

Q1 2 1 0 Q2N2222A \*Tools – Pspice - Library - Bipolar

.MODEL Q2N2222A NPN (IS=2.105E-16 BF=173 VA=83.3V CJE=29.6PF CJC=19.4PF

+ TF=489.88PS TR=4.9NS)

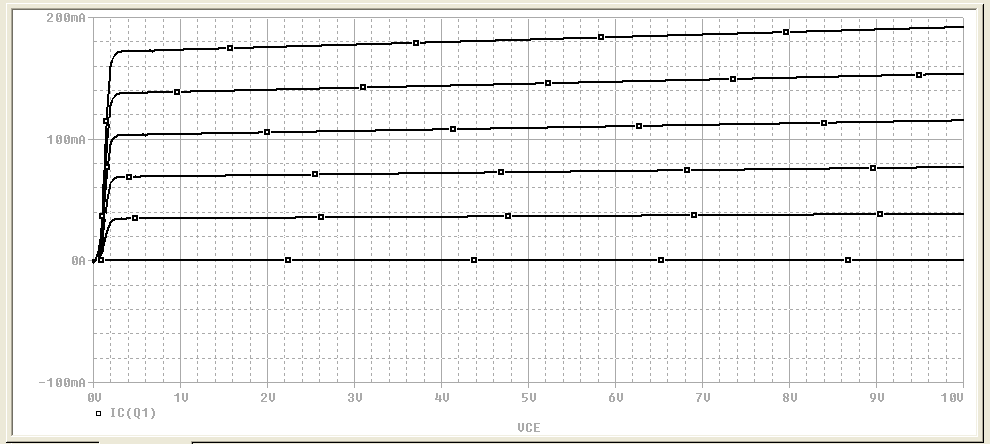
.DC VCE 0 10V 0.02V IB 0 1MA 200UA

.PROBE

.OP

.END

**RESULT:**

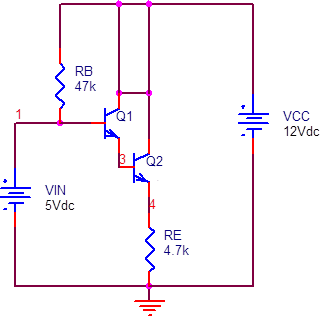


**CONCLUSION:** We are able to visualise the expected output of NPN-BJT circuit as given in theory.

**EXPERIMENT NO 5**

**AIM:** Simulate and study Darlington pair amplifier circuit using PSPICE windows and determine quiescent condition.

**CIRCUIT DIAGRAM:**



**PROGRAM:**

VCC 2 0 DC 12V

VIN 1 0 DC 5V

Q1 2 1 3 Q2N2484 \* BJTs with model (Q2N2484) Q2 2 3 4 Q2N2484

RB 2 1 47k

RE 4 0 4.7K

\* Model Q2N2484 for NPN BJTs

.model Q2N2484 NPN(Is=5.911f Xti=3 Eg=1.11 Vaf=62.37 Bf=697.1 Ne=1.342

+ Ise=5.911f Ikf=13.93m Xtb=1.5 Br=1.297 Nc=2 Isc=0 Ikr=0 Rc=1.61

+ Cjc=4.017p Mjc=.3174 Vjc=.75 Fc=.5 Cje=4.973p Mje=.4146 Vje=.75

+ Tr=4.687n Tf=820.4p Itf=.35 Vtf=4 Xtf=7 Rb=10)

\* Transfer function analysis to calculate dc gain, input resistance and output resistance

.TF V(4) VIN

.END

**RESULT:**

**\*\*\*\* 11/11/13 09:10:06 \*\*\*\*\*\*\* PSpice Lite (April 2011) \*\*\*\*\*\*\* ID# 10813 \*\*\*\***

**\*\*\*\* Darlington Pair**

**\*\*\*\* SMALL SIGNAL BIAS SOLUTION TEMPERATURE = 27.000 DEG C**

**\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE NODE VOLTAGE**

**( 1) 5.0000 ( 2) 12.0000 ( 3) 4.3560 ( 4) 3.5909**

**VOLTAGE SOURCE CURRENTS NAME CURRENT**

**VCC -9.129E-04**

**VIN 1.489E-04**

**TOTAL POWER DISSIPATION 1.02E-02 WATTS**

**\*\*\*\* SMALL-SIGNAL CHARACTERISTICS V(4)/VIN = 9.851E-01**

**INPUT RESISTANCE AT VIN = 4.696E+04 OUTPUT RESISTANCE AT V(4) = 6.677E+01**

**JOB CONCLUDED**

**\*\*\*\* 11/11/13 09:10:06 \*\*\*\*\*\*\* PSpice Lite (April 2011) \*\*\*\*\*\*\* ID# 10813 \*\*\*\***

**\*\*\*\* Darlington Pair**

**\*\*\*\* JOB STATISTICS SUMMARY**

**\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\*\* Total job time (using Solver 1) = 0.00**

**EXPERIMENT NO 6**

**AIM:** Simulate and study transient & frequency response of a BJT amplifier in common- emitter configuration using PSPICE windows.

**CIRCUIT DIAGRAM:**

Vcc 15Vdc



RC

R1

47k

10k

C2

4

6

Rs

1 2

500

C1

10uF

3

Q1

10uF

Q2N2907

5

VIN

R2

5k

RL

20k

RE

2k

CE

10uF

VOFF = 0 VAMPL = 10mV FREQ = 1kHz

**PROGRAM:**

\*

.AC DEC 10 1hz 10khz;

VIN 1 0 AC 10mv sin(0 10mv 1khz); VCC 0 7 DC 15v;

RS 1 2 500;

R1 7 3 47k;

R2 3 0 5k;

RC 7 4 10k;

RE 5 0 2k;

RL 6 0 20k;

C1 2 3 10uF;

C2 4 6 10uF;

CE 5 0 10uF;

Q1 4 3 5 0 Q2N2907;

.model Q2N2907 PNP(Is=650.6E-18 Xti=3 Eg=1.11 Vaf=115.7 Bf=231.7 Ne=1.829

+ Ise=54.81f Ikf=1.079 Xtb=1.5 Br=3.563 Nc=2 Isc=0 Ikr=0 Rc=.715

+ Cjc=14.76p Mjc=.5383 Vjc=.75 Fc=.5 Cje=19.82p Mje=.3357 Vje=.75

+ Tr=111.3n Tf=603.7p Itf=.65 Vtf=5 Xtf=1.7 Rb=10)

* National pid=63 case=TO18
* 88-09-09 bam creation

.tran 50us 2ms;

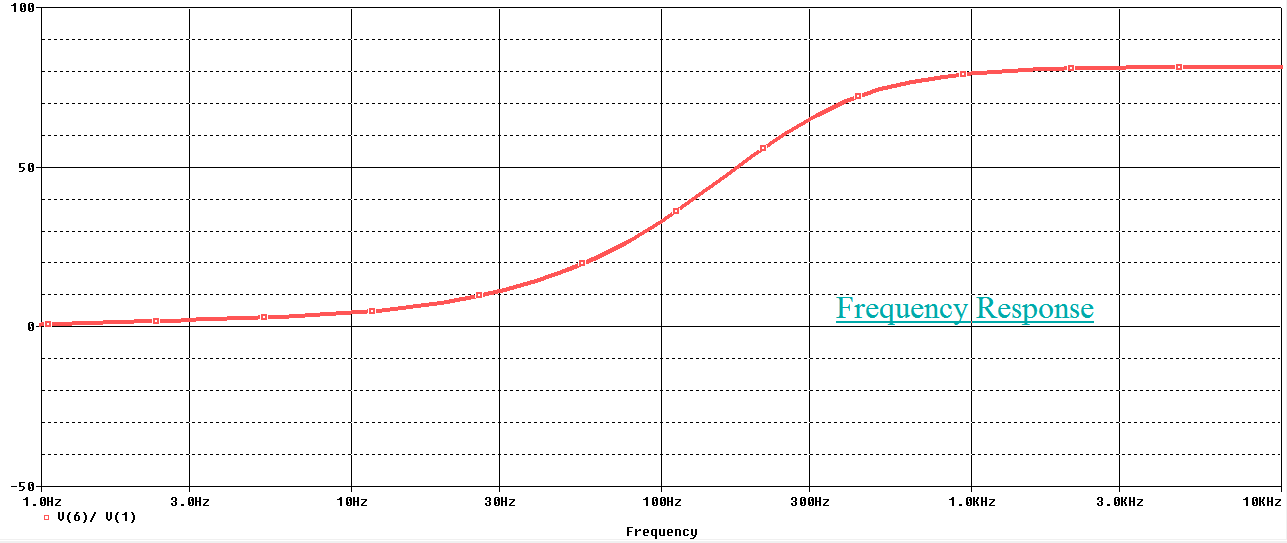
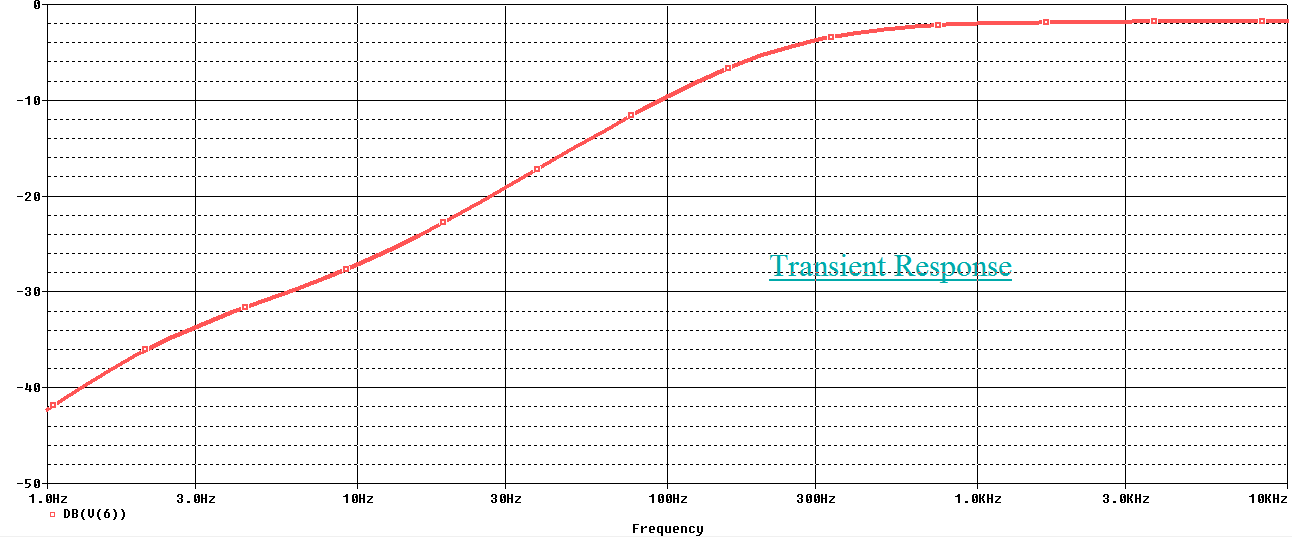
.plot tran V(4) V(6) V(1);

.plot AC VM(6) VP(6);

.probe;

.end;

**RESULT:**



**CONCLUSION:** We are able to visualise the expected output of transient & frequency response of a BJT amplifier in common-emitter configuration as given in theory.

**EXPERIMENT NO 7**

**AIM:** Simulate and study active low-pass, high-pass & band-pass filter using PSPICE windows.

**CIRCUIT DIAGRAM:**

RG RF

### Low-pass Filter

10k

100k

3 +

OUT

1

Vo

R1

2 -

UA741

8

~~V~~-

V+

C1

10k

Vin

4

0.1uF

R4

### High-pass Filter

10k

R2

20k C2

1n

R1

3 + 20k

R5

OUT

1

Vo

2

10k

V1

-

UA741

R3

10k

4

8

V-

V+

R4

10k R2

R1

3 + 20k

2

-

V1

~~V~~-

20k C2

1n

8

V+

OUT 1

R5

10k

3 +

8

OUT 1

V+

### Band-pass Filter

Vo

UA741

4

R3

2 -

UA741

~~V~~-

10k R6

4

100k

R7

100k

## PROGRAM:

\*Low Pass Filter (BY UA 741) VIN 1 0 AC 1

RG 3 0 10K

RF 3 4 100K

R1 1 2 15.9K

C1 2 0 .01UF

XA1 2 3 7 4 6 UA741

\*-----------------------------------------------------------------------------

* connections: non-inverting input
* | inverting input
* | | positive power supply
* | | | negative power supply
* | | | | output

\* | | | | |

.subckt uA741 1 2 3 4 5

\* c1 11 12 8.661E-12

c2 6 7 30.00E-12

dc 5 53 dy

de 54 5 dy

dlp 90 91 dx

dln 92 90 dx

dp 4 3 dx

egnd 99 0 poly(2),(3,0),(4,0) 0 .5 .5

fb 7 99 poly(5) vb vc ve vlp vln 0 10.61E6 -1E3 1E3 10E6 -10E6 ga 6 0 11 12 188.5E-6

gcm 0 6 10 99 5.961E-9

iee 10 4 dc 15.16E-6

hlim 90 0 vlim 1K

q1 11 2 13 qx

q2 12 1 14 qx

r2 6 9 100.0E3

rc1 3 11 5.305E3

rc2 3 12 5.305E3

re1 13 10 1.836E3

re2 14 10 1.836E3

ree 10 99 13.19E6

ro1 8 5 50

ro2 7 99 100

rp 3 4 18.16E3

vb 9 0 dc 0

vc 3 53 dc 1

ve 54 4 dc 1

vlim 7 8 dc 0

vlp 91 0 dc 40

vln 0 92 dc 40

.model dx D(Is=800.0E-18 Rs=1)

.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)

.model qx NPN(Is=800.0E-18 Bf=93.75)

.ends

.AC DEC 10 10HZ 100GHZ

.PLOT AC VM(4) VP(4)

.PROBE

.END

* HIGH PASS Filter (BY UA741) VIN 1 0 AC 1

RG 3 0 10K

RF 3 4 10K

C1 1 2 .01UF

R1 2 0 15.9K

XA1 2 3 7 4 6 UA741

\*-----------------------------------------------------------------------------

* connections: non-inverting input
* | inverting input
* | | positive power supply
* | | | negative power supply
* | | | | output

\* | | | | |

.subckt uA741 1 2 3 4 5

\*

c1 11 12 8.661E-12

c2 6 7 30.00E-12

dc 5 53 dy

de 54 5 dy

dlp 90 91 dx

dln 92 90 dx

dp 4 3 dx

egnd 99 0 poly(2),(3,0),(4,0) 0 .5 .5

fb 7 99 poly(5) vb vc ve vlp vln 0 10.61E6 -1E3 1E3 10E6 -10E6 ga 6 0 11 12 188.5E-6

gcm 0 6 10 99 5.961E-9

iee 10 4 dc 15.16E-6

hlim 90 0 vlim 1K

q1 11 2 13 qx

q2 12 1 14 qx

r2 6 9 100.0E3

rc1 3 11 5.305E3

rc2 3 12 5.305E3

re1 13 10 1.836E3

re2 14 10 1.836E3

ree 10 99 13.19E6

ro1 8 5 50

ro2 7 99 100

rp 3 4 18.16E3

vb 9 0 dc 0

vc 3 53 dc 1

ve 54 4 dc 1

vlim 7 8 dc 0

vlp 91 0 dc 40

vln 0 92 dc 40

.model dx D(Is=800.0E-18 Rs=1)

.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)

.model qx NPN(Is=800.0E-18 Bf=93.75)

.ends

.AC DEC 10 10HZ 100KHZ

.PLOT AC VM(4) VP(4)

.PROBE

.END

\*BAND PASS FILTER VIN 1 0 AC 1V

R1 1 2 5K

R2 3 4 1.5K

R3 2 0 265K

C1 2 4 0.01UF

C2 2 3 0.01UF

RL 4 0 15K

VCC 6 0 DC 12V

VEE 0 7 DC 12V

XA1 0 3 6 7 4 UA741

.subckt uA741 1 2 3 4 5

\*

c1 11 12 8.661E-12

c2 6 7 30.00E-12

dc 5 53 dy

de 54 5 dy

dlp 90 91 dx

dln 92 90 dx

dp 4 3 dx

egnd 99 0 poly(2),(3,0),(4,0) 0 .5 .5

fb 7 99 poly(5) vb vc ve vlp vln 0 10.61E6 -1E3 1E3 10E6 -10E6 ga 6 0 11 12 188.5E-6

gcm 0 6 10 99 5.961E-9

iee 10 4 dc 15.16E-6

hlim 90 0 vlim 1K

q1 11 2 13 qx

q2 12 1 14 qx

r2 6 9 100.0E3

rc1 3 11 5.305E3

rc2 3 12 5.305E3

re1 13 10 1.836E3

re2 14 10 1.836E3

ree 10 99 13.19E6

ro1 8 5 50

ro2 7 99 100

rp 3 4 18.16E3

vb 9 0 dc 0

vc 3 53 dc 1

ve 54 4 dc 1

vlim 7 8 dc 0

vlp 91 0 dc 40

vln 0 92 dc 40

.model dx D(Is=800.0E-18 Rs=1)

.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)

.model qx NPN(Is=800.0E-18 Bf=93.75)

.ends

.AC DEC 10 100HZ 1MEGHZ

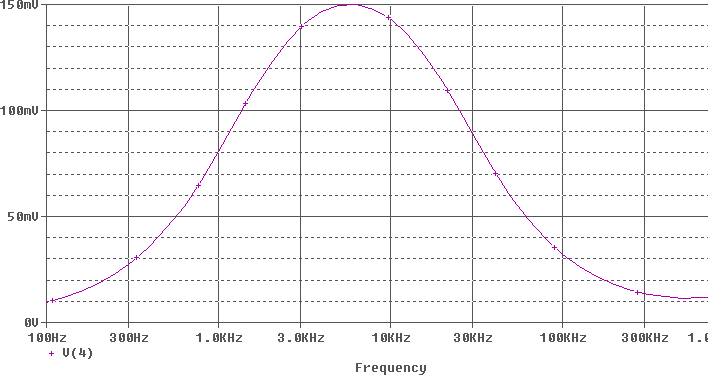
.PLOT AC VM(4) VP(4)

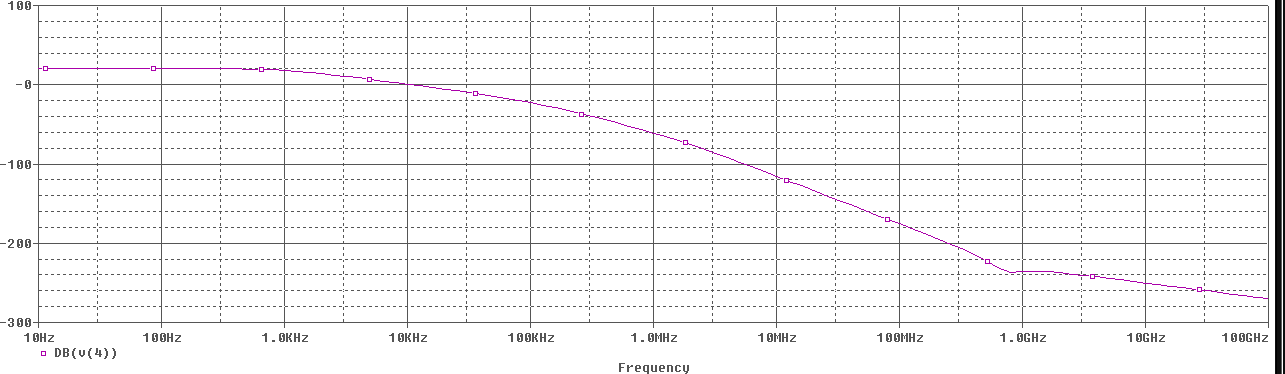
.PROBE

.END

## RESULT:

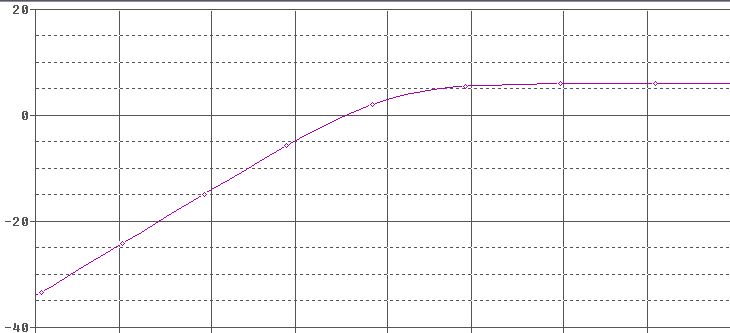
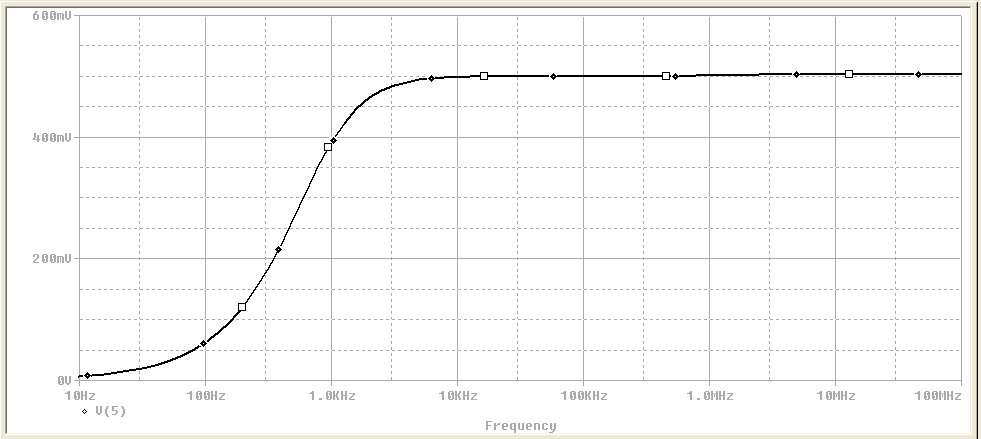
\*LOW PASS CIRCUIT





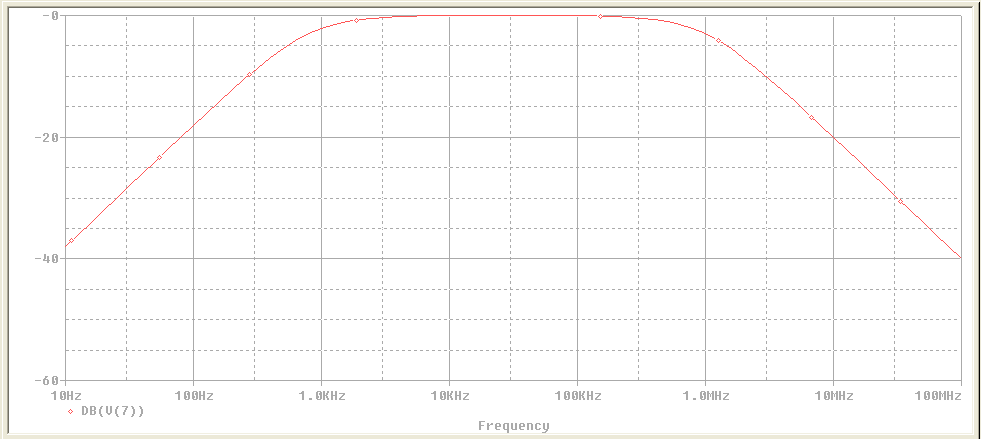
**RESULT:**

\*HIGH PASS CIRCUIT



\*BAND PASS CIRCUIT





**CONCLUSION:** We are able to visualise the expected output of active low-pass, high-pass & band-pass filter as given in theory.

**EXPERIMENT NO 8**

**AIM:** Simulate and study Integrator using PSPICE windows.

**CIRCUIT DIAGRAM:** C1

R1

1 2

Vin

2.5k

0.1uF

Rf

4

1MEG

8

3 +

V+

OUT 1

output voltage

3 2 -

V-

Rx

4

2.5k

Rl

100k

## PROGRAM:

\* INTEGRATOR

VIN 1 0 PWL(0 0 1NS -1V 1MS -1V 1.0001MS 1v 2ms 1v 2.0001ms -1V 3MS -1V 3.0001MS 1V 4MS 1V)

R1 1 3 2.5K

RF 3 6 1MEG

RX 2 0 2.5K

RL 6 0 100K

C1 3 6 0.1UF

XA1 2 3 7 4 6 UA741

\*-----------------------------------------------------------------------------

* connections: non-inverting input
* | inverting input
* | | positive power supply
* | | | negative power supply
* | | | | output

\* | | | | |

.subckt uA741 1 2 3 4 5

\*

c1 11 12 8.661E-12

c2 6 7 30.00E-12

dc 5 53 dy

de 54 5 dy

dlp 90 91 dx

dln 92 90 dx

dp 4 3 dx

egnd 99 0 poly(2),(3,0),(4,0) 0 .5 .5

fb 7 99 poly(5) vb vc ve vlp vln 0 10.61E6 -1E3 1E3 10E6 -10E6 ga 6 0 11 12 188.5E-6

gcm 0 6 10 99 5.961E-9

iee 10 4 dc 15.16E-6

hlim 90 0 vlim 1K

q1 11 2 13 qx

q2 12 1 14 qx

r2 6 9 100.0E3

rc1 3 11 5.305E3

rc2 3 12 5.305E3

re1 13 10 1.836E3

re2 14 10 1.836E3

ree 10 99 13.19E6

ro1 8 5 50

ro2 7 99 100

rp 3 4 18.16E3

vb 9 0 dc 0

vc 3 53 dc 1

ve 54 4 dc 1

vlim 7 8 dc 0

vlp 91 0 dc 40

vln 0 92 dc 40

.model dx D(Is=800.0E-18 Rs=1)

.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)

.model qx NPN(Is=800.0E-18 Bf=93.75)

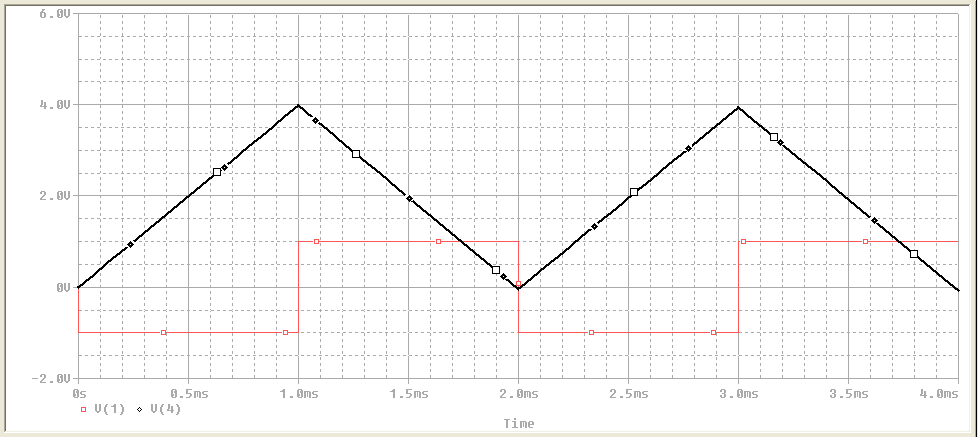
.ends

.TRAN 50US 4MS

.PROBE

.END

## RESULT:



**CONCLUSION:** We are able to visualise the expected output of Integrator circuit as given in theory.

**EXPERIMENT NO 9**

**AIM:** Simulate and study Differentiator using PSPICE windows.

**CIRCUIT DIAGRAM:**

R1 C1

1 2 3



100

Vin

0.4uF

Rf

4

10k

3 +

8

V+

OUT 1

5 2 -

V-

output voltage

Rx

4

10k

Rl

100k

## PROGRAM:

\*DIFFERENTIATOR CIRCUIT

VIN 1 0 PWL(0 0 1MS 1 2MS 0 3MS 1 4MS 0)

R1 1 8 82

RF 3 6 1.5K

RX 2 0 1.5K

RL 6 0 10K

C1 8 3 0.1UF

CF 3 6 .005UF

XA1 2 3 7 4 6 UA741

\*-----------------------------------------------------------------------------

* connections: non-inverting input
* | inverting input
* | | positive power supply
* | | | negative power supply
* | | | | output

\* | | | | |

.subckt uA741 1 2 3 4 5

\*

c1 11 12 8.661E-12

c2 6 7 30.00E-12

dc 5 53 dy

de 54 5 dy

dlp 90 91 dx

dln 92 90 dx

dp 4 3 dx

egnd 99 0 poly(2),(3,0),(4,0) 0 .5 .5

fb 7 99 poly(5) vb vc ve vlp vln 0 10.61E6 -1E3 1E3 10E6 -10E6 ga 6 0 11 12 188.5E-6

gcm 0 6 10 99 5.961E-9

iee 10 4 dc 15.16E-6

hlim 90 0 vlim 1K

q1 11 2 13 qx

q2 12 1 14 qx

r2 6 9 100.0E3

rc1 3 11 5.305E3

rc2 3 12 5.305E3

re1 13 10 1.836E3

re2 14 10 1.836E3

ree 10 99 13.19E6

ro1 8 5 50

ro2 7 99 100

rp 3 4 18.16E3

vb 9 0 dc 0

vc 3 53 dc 1

ve 54 4 dc 1

vlim 7 8 dc 0

vlp 91 0 dc 40

vln 0 92 dc 40

.model dx D(Is=800.0E-18 Rs=1)

.model dy D(Is=800.00E-18 Rs=1m Cjo=10p)

.model qx NPN(Is=800.0E-18 Bf=93.75)

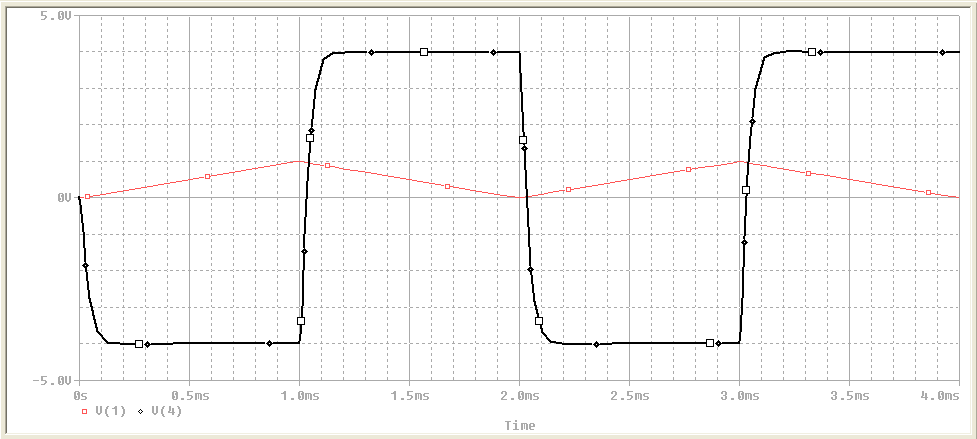
.ends

.TRAN 50US 4MS

.PROBE

.END

## RESULT:



**CONCLUSION:** We are able to visualise the expected output of Differentiator circuit as given in theory.

**EXPERIMENT NO.10**

**AIM:** Simulate and study basic AND, OR, NOT, NOR, NAND, EX-OR gates using PSPICE windows.

**CIRCUIT DIAGRAM:**

**AND GATE**

OFFTIME = .2uSDSTM1 ONTIME = .5uS

CLK

V

U1

1

3

2

AND2

DELAY = 0

STARTVAL = 0

OPPVAL = 1

OFFTIME = .5uSDSTM2

## NAND GATE

OFFTIME = .2uSDSTM3 ONTIME = .5uS CLK DELAY = 0

STARTVAL = 0

OPPVAL = 1

V

U5

1

3

2

NAN2 V

ONTIME = .2uS DELAY = 0

STARTVAL = 0

OPPVAL = 1

## OR GATE

CLK

V

OFFTIME = .3uSDSTM4 ONTIME = .1uS CLK DELAY = 0

STARTVAL = 0

OPPVAL = 1

## NOR GATE

OFFTIME = .2uSDSTM3 ONTIME = .5uS CLK



DELAY = 0

STARTVAL = 0

OPPVAL = 1

U6

1

3

2

OFFTIME = .2uSDSTM3 ONTIME = .5uS CLK

DELAY = 0



STARTVAL = 0

OPPVAL = 1

U4

OR2 V 1 3

2

OFFTIME = .3uSDSTM4 ONTIME = .1uS CLK

DELAY = 0

STARTVAL = 0

OPPVAL = 1

## NOT GATE

OFFTIME = .3uSDSTM4 ONTIME = .1uS CLK

DELAY = 0

STARTVAL = 0

OPPVAL = 1

NOR2 V

OFFTIME = .2uSDSTM3 ONTIME = .5uS

CLK

V

1

DELAY = 0

STARTVAL = 0

OPPVAL = 1

## NOR GATE

U9

2

INV

V

OFFTIME = .2uSDSTM3 ONTIME = .5uS CLK



DELAY = 0

STARTVAL = 0

OPPVAL = 1

U7

1

3

2

XOR V

OFFTIME = .3uSDSTM4 ONTIME = .1uS CLK

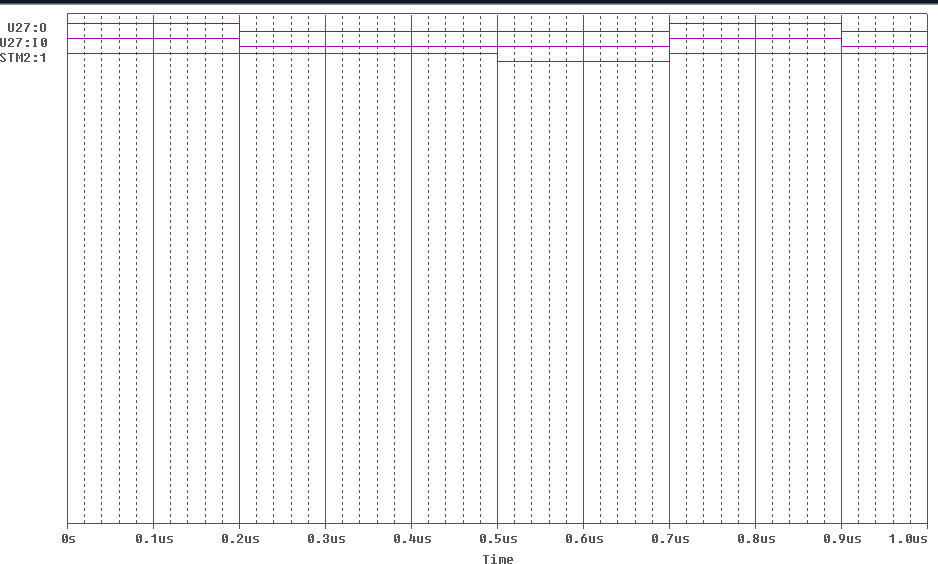
DELAY = 0

STARTVAL = 0

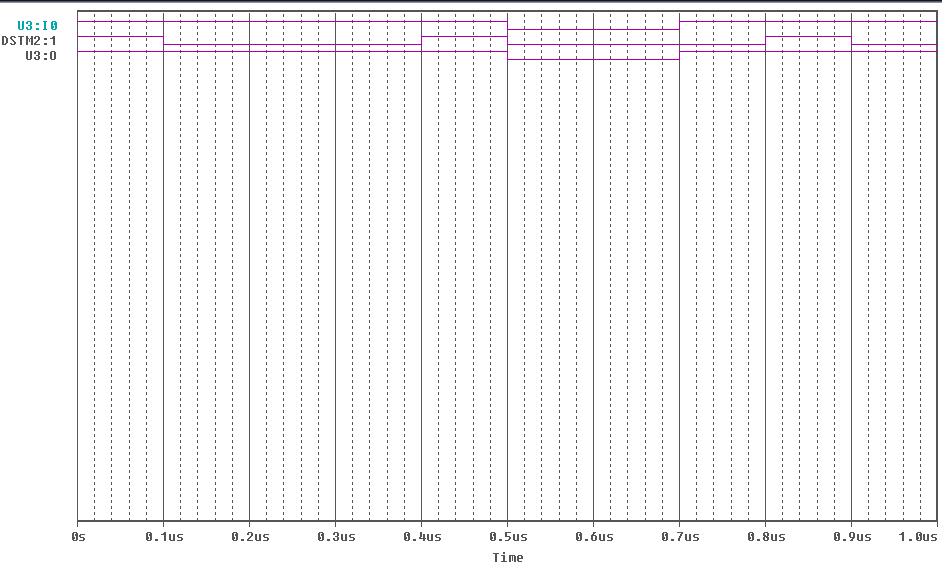
OPPVAL = 1

## OUTPUT:

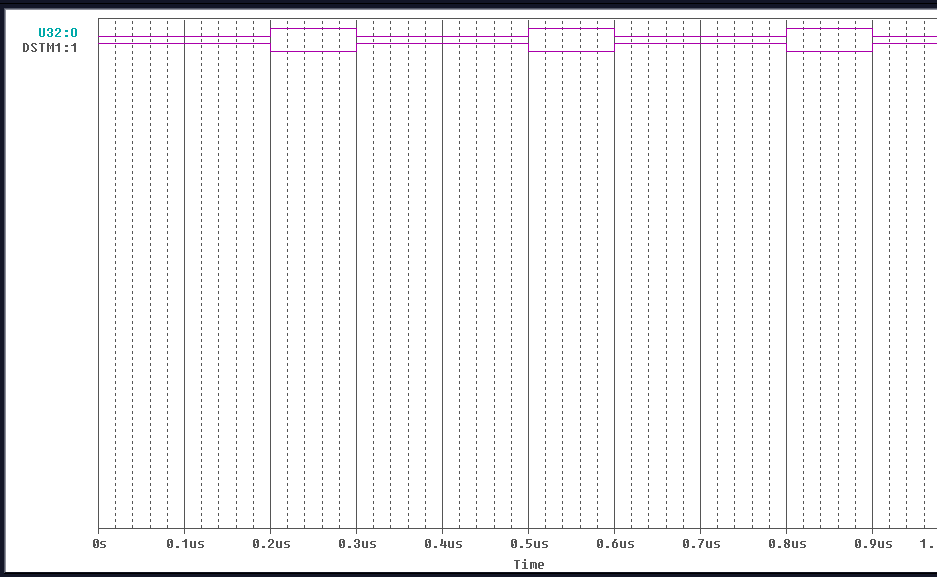
1. **AND GATE**



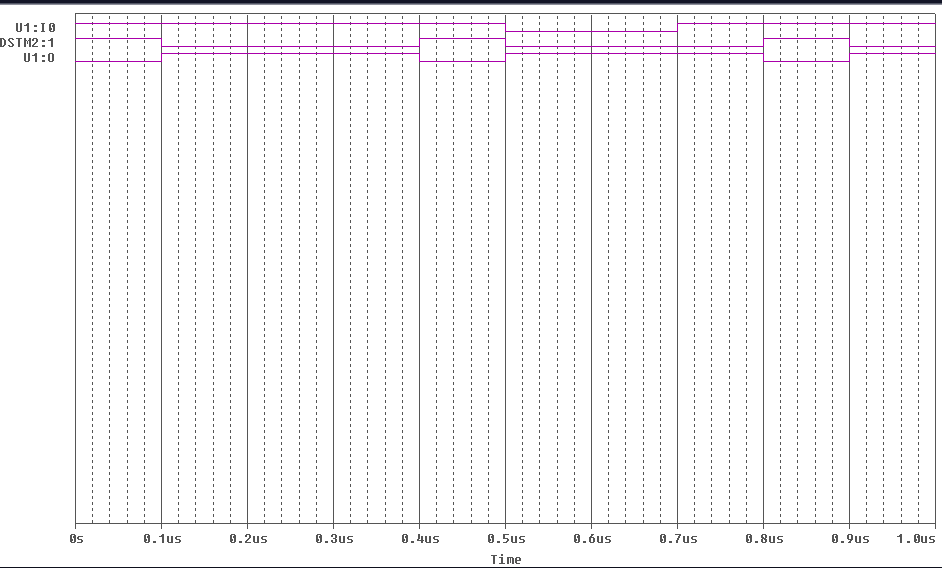
1. **OR GATE**



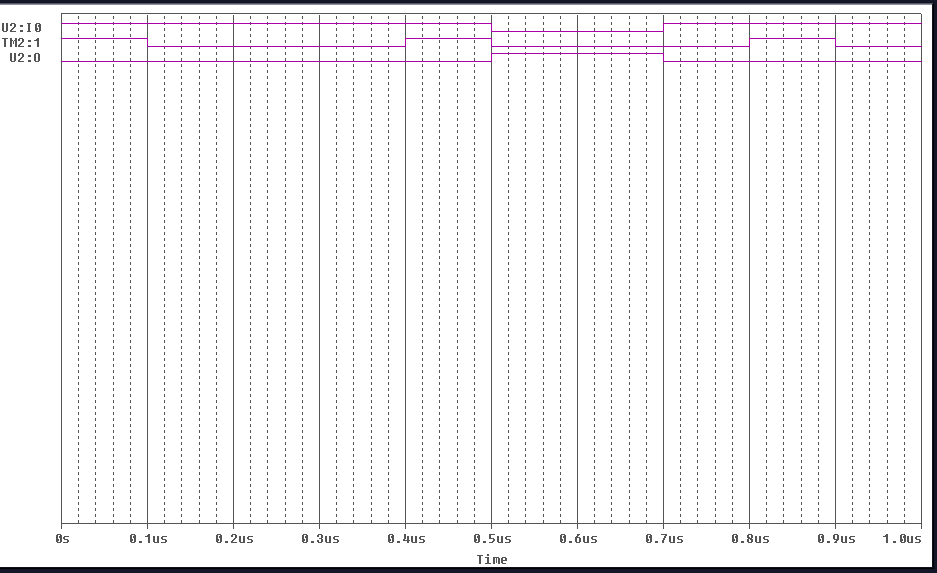
1. **NOT GATE**



1. **NAND GATE**



1. **NOR GATE**



1. **X-OR GATE**

